CLAIMS

What is claimed is:

1. A unidirectional low capacitance transient voltage suppressor ("TVS"), comprising:

a TVS p-n junction diode element;

a low-capacitance ("LC") PIN or NIP diode element; and

the TVS p-n junction diode element being placed in series with opposite polarity to LC PIN diode.

2. The circuit of Claim 1, wherein the PIN or NIP diode has an intrinsic "I" region of high resistivity with a long lifetime;

a highly doped p region;

an n region; and

the "I" region is located between the p region and n region.

3. The circuit of Claim 2, wherein the "I" region of the PIN or NIP diode has a width of between 10 and 500 μm and a resistivity of 250 ohm-cm or higher.

4. The circuit of Claim 2, wherein the PIN or NIP diode has a circular-die structure.

5. The circuit of Claim 2, wherein the PIN or NIP diode has a square die structure.

6. The circuit of Claim 2, wherein the PIN or NIP diode has a rectangular die structure.

7. The circuit of Claim 1, adapted to clamp high-voltage transients of either polarity to a predetermined level.

8. The circuit of Claim 1, wherein the use of the PIN or NIP diode minimizes parasitic losses and signal-line distortion.

9. The circuit of Claim 1, adapted to provide low capacitance, low voltage clamping and minimal capacitance variation.

10. The circuit of Claim 9, operable to reduce the complexity of impedance matching within a high frequency circuit.

11. The circuit of Claim 9, operable to lower the clamping voltage performance of TVS with capacitances in the range of about 1 pF to 100 pF.

12. The circuit of Claim 1, in combination with a low parasitic package, operable to reduce capacitances to less than 1 pF.

13. The circuit of Claim 1, for use in multiple diode arrays.

14. The circuit of Claim 1, further comprising a TVS array packaged in a SOIC-8 package.

15. The circuit of Claim 1, further comprising a TVS array packaged in an eight (8) pin dual-in-line package.

16. The circuit of Claim 1, further comprising a TVS array packaged in a SOIC-14 package.

17. The circuit of Claim 1, further comprising a TVS array packaged in a fourteen (14) pin dual-in-line package.

18. The circuit of Claim 1, further comprising a TVS array provided in multiple discrete semiconductor chips.

19. The circuit of Claim 1, further comprising a TVS array using multiple diode junctions diffused into a single semiconductor chip or monolithic structure.

20. The circuit of Claim 1, further comprising a TVS array using three (3) or more terminal packages containing multiple diodes within a single package where at least one of the diodes is a TVS.

21. The circuit of Claim 1, adapted for use in high frequency telecommunication lines.

22. The circuit of Claim 1, adapted for use in wireless communications devices.

23. The circuit of Claim 1, adapted for use in high baud-rate lines requiring TVS protection.

24. The circuit of Claim 1, adapted for use in multimedia systems.

25. The circuit of Claim 1, adapted for use in network applications and system designs.

26. A bi-directional low capacitance transient voltage suppressor ("TVS") protection circuit, comprising:

a first and second TVS diode;

a first and second low-capacitance ("LC") PIN or NIP diode;

the first TVS diode being placed in series with opposite polarity to the first LC PIN or NIP diode;

the second TVS diode being placed in series with opposite polarity to the second LC PIN or NIP diode; and

the first series connected TVS diode and LC PIN or NIP diode being arranged parallel, and in the opposite direction, to the second series connected TVS diode and LC PIN or NIP diode.

27. The circuit of Claim 26, wherein each of the PIN or NIP diodes have an intrinsic "I" region of high resistivity with a long lifetime;

a highly doped p region;

an n region; and

the "I" region being located between the p region and the n region.

28. The circuit of Claim 26, wherein the "I" region of each of the PIN or NIP diodes have a width of between 10 and 500 μm and a resistivity of 250 ohm-cm or higher.

29. The circuit of Claim 26, wherein the PIN or NIP diodes have a circular-die structure.

30. The circuit of Claim 26, wherein the PIN or NIP diodes have a square die structure.

31. The circuit of Claim 26, wherein the PIN or NIP diodes have a rectangular die structure.

32. The circuit of Claim 26, adapted to clamp high-voltage transients of either polarity to a predetermined level.

33. The circuit of Claim 26, wherein the use of the PIN or NIP diodes minimize parasitic losses and signal-line distortion.

34. The circuit of Claim 26, adapted to provide low capacitance, low voltage clamping and minimal capacitance variation.

35. The circuit of Claim 34, operable to reduce the complexity of impedance matching within a high frequency circuit.

36. The circuit of Claim 26, operable to lower the clamping voltage performance of TVS with capacitances in the range of about 1 pF to 100 pF.

37. The circuit of Claim 26, in combination with low parasitic packages operable to reduce capacitances to less than 1 pF.

38. The circuit of Claim 26, for use in multiple diode arrays.

39. The circuit of Claim 26, further comprising a TVS array packaged in a SOIC-8

package.

40. The circuit of Claim 26, further comprising a TVS array packaged in an eight (8) pin dual-in-line package.

41. The circuit of Claim 26, further comprising a TVS array packaged in a SOIC-14 package.

42. The circuit of Claim 26, further comprising a TVS array packaged in an fourteen (14) pin dual-in-line package.

43. The circuit of Claim 26, further comprising a TVS array provided in multiple discrete semiconductor chips.

44. The circuit of Claim 26, further comprising a TVS array using multiple diode junctions diffused into a single semiconductor chip or monolithic structure.

45. The circuit of Claim 26, further comprising a TVS array packaged with three (3) or more terminals.

46. The circuit of Claim 26 adapted for use in high frequency telecommunication lines.

47. The circuit of Claim 26 adapted for use in wireless communications devices.

48. The circuit of Claim 26 adapted for use in high baud-rate lines requiring TVS protection.

49. The circuit of Claim 26 adapted for use in multimedia systems.

50. The circuit of Claim 26 adapted for use in network applications and system designs.

51. A unidirectional, low capacitance transient voltage suppressor ("TVS") protection circuit, comprising:

a TVS diode;

a first and second low-capacitance ("LC") PIN or NIP diode;

the TVS diode being placed in series with opposite polarity to the first LC PIN or NIP diode; and

the series connected TVS diode and first LC PIN or NIP diode being arranged parallel to, and in the opposite direction, to the second LC PIN or NIP diode.

52. The circuit of Claim 51, wherein each of the PIN or NIP diodes has an intrinsic "I" region of high resistivity with a long lifetime;

a highly doped p region;

an n region;

the "I" region being located between the p region and n region.

53. The circuit of Claim 52 wherein the "I" region of each of the PIN or NIP diodes has a width of between 10 and 500 μm and a resistivity of 250 ohm-cm or higher.

54. The circuit of Claim 52, adapted to clamp high-voltage transients of either polarity to a predetermined level.

55. The circuit of Claim 52, wherein the use of PIN or NIP diodes minimize parasitic losses and signal-line distortion.

56. The circuit of Claim 52, adapted to provide low capacitance, low voltage clamping and minimal capacitance variation.

57. The circuit of Claim 52, operable to reduce the complexity of impedance matching within a high frequency circuit.

58. The circuit of Claim 52, operable to lower the clamping voltage performance of TVS with capacitances in the range of about 1 pF to 100 pF.

59. The circuit of Claim 52, in combination with low parasitic packages operable to reduce capacitances to less than 1 pF.

60. The circuit of Claim 52, for use in multiple diode arrays.

61. The circuit of Claim 52, wherein the TVS array is packaged in a SOIC-8 package.

62. The circuit of Claim 52, wherein the TVS array is packaged in an eight (8) pin dual-in-line package.

63. The circuit of Claim 52, wherein the TVS array is packaged in a SOIC-14 package.

64. The circuit of Claim 52, wherein the TVS array is packaged in an fourteen (14) pin dual-in-line package.

65. The circuit of Claim 52, wherein the TVS array is provided in multiple discrete semiconductor chips.

66. The circuit of Claim 52, wherein the TVS array is provided using multiple diode junctions diffused into a single semiconductor chip or monolithic structure.

67. The circuit of Claim 52, further comprising a TVS array packaged with three (3) or more terminals.

68. The circuit of Claim 52, adapted for use in high frequency telecommunication lines.

69. The circuit of Claim 52, adapted for use in wireless communications.

70. The circuit of Claim 52, adapted for use in high baud-rate lines requiring TVS protection.

71. The circuit of Claim 52, adapted for use in multimedia systems.

72. The circuit of Claim 52, adapted for use in network applications and system designs.

73. A circuit arrangement to protect a signal line or input/output (I/O) port, comprising:

a first PIN or NIP steering diode with a cathode and anode;

a second PIN or NIP steering diode with a cathode and anode;

the anode of the first PIN or NIP steering diode coupled to a signal line or input/output (I/O) port;

the cathode of the first PIN or NIP steering diode coupled to a positive power supply line;

the cathode of the second PIN or NIP steering diode coupled to a signal line or input/output (I/O) port; and

the anode of the second PIN or NIP steering diode coupled to ground or a negative power supply line.

74. The circuit of Claim 73, adapted to clamp high-voltage transients of either polarity to a predetermined level.

75. The circuit of Claim 73, wherein the use of PIN or NIP steering diodes minimize parasitic losses and signal-line distortion.

76. The circuit of Claim 73, adapted to provide low capacitance, low voltage clamping and minimal capacitance variation.

77. The circuit of Claim 73, operable to reduce the complexity of impedance matching within a high frequency circuit.

78. The circuit of Claim 73, operable to lower the clamping voltage performance of TVS with capacitances in the range of about 1 pF to 100 pF.

79. The circuit of Claim 73, in combination with low parasitic packages operable to reduce capacitances to less than 1 pF.

80. The circuit of Claim 73, wherein the PIN or NIP steering diodes have an intrinsic "I" region of high resistivity with a long lifetime;

a highly doped p region;

an n region;

the "I" region is located between the p region and n region.

81. The circuit of Claim 80 wherein the "I" region of the PIN or NIP steering diodes have a width of between 10 and 500 μm and a resistivity of 250 ohm-cm or higher.

82. The circuit of Claim 80, wherein the PIN or NIP diode has a circular-die structure.

83. The circuit of Claim 80, wherein the PIN or NIP diode has a square die structure.

84. The circuit of Claim 80, wherein the PIN or NIP diode has a rectangular die structure.

85. The circuit of Claim 73, for use in multiple diode-leg arrays.

86. The circuit of Claim 73, comprising a PIN or NIP diode array packaged in a SOIC-8 package.

87. The circuit of Claim 73, comprising a PIN or NIP diode array packaged in an eight (8) pin dual-in-line package.

88. The circuit of Claim 73, comprising a PIN or NIP diode array packaged in a SOIC-14 package.

89. The circuit of Claim 73, comprising a PIN or NIP diode array packaged in a fourteen (14) pin dual-in-line package.

90. The circuit of Claim 73, comprising a PIN or NIP diode array provided in multiple discrete semiconductor chips.

91. The circuit of Claim 73, comprising a PIN or NIP diode array provided using multiple diode junctions diffused into a single semiconductor chip or monolithic structure.

92. The circuit of Claim 73, further comprising a TVS array packaged with three (3) or more terminals.

93. The circuit of Claim 73, adapted for use in high frequency telecommunication lines.

94. The circuit of Claim 73, adapted for use in wireless communications devices.

95. The circuit of Claim 73, adapted for use in high baud-rate lines requiring TVS protection.

96. The circuit of Claim 73, adapted for use in multimedia systems.

97. The circuit of Claim 73, adapted for use in network applications and system designs.

98. A method of protecting sensitive components downstream in the circuit, comprising:

using TVS diodes and PIN or NIP diodes to clamp voltages at a point upstream from

sensitive components to a predetermined level;

shunting high-voltage transients to ground or to other reference points such as the positive ($+V_{CC}$) or negative ($-V_{CC}$) side of a power-supply line.

minimizing capacitance variations with applied reverse voltage across the PIN or NIP diodes.

99. A circuit arrangement to protect a signal line or input/output (I/O) port, comprising:

an individual PIN or NIP steering diode with a cathode and anode;

the anode of the PIN or NIP steering diode coupled to a signal line or input/output (I/O) port; and

the cathode of the PIN or NIP steering diode coupled to a line with higher voltage (Vcc) relative to the signal line or input/output (I/O) port.

100. The circuit of Claim 99, adapted to clamp high-voltage transients of either polarity to a predetermined level.

101. The circuit of Claim 99, wherein the use of PIN or NIP steering diodes minimize parasitic losses and signal-line distortion.

102. The circuit of Claim 99, adapted to provide low capacitance, low voltage clamping and minimal capacitance variation.

103. The circuit of Claim 99, operable to reduce the complexity of impedance matching within a high frequency circuit.

104. The circuit of Claim 99, operable to lower the clamping voltage performance with capacitances in the range of about 1 pF to 100 pF.

105. The circuit of Claim 99, in combination with low parasitic packages operable to reduce capacitances to less than 1 pF.

106. The circuit of Claim 99, wherein the PIN or NIP steering diodes have an intrinsic "I" region of high resistivity with a long lifetime;

a highly doped p region;

an n region;

the "I" region is located between the p region and n region.

107. The circuit of Claim 106 wherein the "I" region of the PIN or NIP steering diodes have a width of between 10 and 500 μm and a resistivity of 250 ohm-cm or higher.

108. The circuit of Claim 106, wherein the PIN or NIP diode has a circular-die structure.

109. The circuit of Claim 106, wherein the PIN or NIP diode has a square die structure.

110. The circuit of Claim 106, wherein the PIN or NIP diode has a rectangular die structure.

111. The circuit of Claim 99, for use in multiple diode-leg arrays.

112. The circuit of Claim 99, comprising a PIN or NIP diode array packaged in a SOIC-8 package.

113. The circuit of Claim 99, comprising a PIN or NIP diode array packaged in an eight (8) pin dual-in-line package.

114. The circuit of Claim 99, comprising a PIN or NIP diode array packaged in a SOIC-14 package.

115. The circuit of Claim 99, comprising a PIN or NIP diode array packaged in a fourteen (14) pin dual-in-line package.

116. The circuit of Claim 99, comprising a PIN or NIP diode array provided in multiple discrete semiconductor chips.

117. The circuit of Claim 99, comprising a PIN or NIP diode array provided using multiple diode junctions diffused into a single semiconductor chip or monolithic structure.

118. The circuit of Claim 99, further comprising an array packaged with three (3) or more terminals.

119. The circuit of Claim 99, adapted for use in high frequency telecommunication lines.

120. The circuit of Claim 99, adapted for use in wireless communications devices.

121. The circuit of Claim 99, adapted for use in high baud-rate lines requiring TVS protection.

122. The circuit of Claim 99, adapted for use in multimedia systems.

123. The circuit of Claim 99, adapted for use in network applications and system designs.

124. A circuit arrangement to protect a signal line or input/output (I/O) port, comprising:

an individual PIN or NIP steering diode with a cathode and anode;

the cathode of the PIN or NIP steering diode coupled to a signal line or input/output (I/O) port; and;

the anode of the PIN or NIP steering diode coupled to a line with lower voltage (-Vcc) or ground relative to the signal line or input/output (I/O) port.

125. The circuit of Claim 124, adapted to clamp high-voltage transients of either polarity to a predetermined level.

126. The circuit of Claim 125, wherein the use of PIN or NIP steering diodes minimize parasitic losses and signal-line distortion.

127. The circuit of Claim 124, adapted to provide low capacitance, low voltage clamping and minimal capacitance variation.

128. The circuit of Claim 124, operable to reduce the complexity of impedance matching within a high frequency circuit.

129. The circuit of Claim 124, operable to lower the clamping voltage performance with capacitances in the range of about 1 pF to 100 pF.

130. The circuit of Claim 124, in combination with low parasitic packages operable to reduce capacitances to less than 1 pF.

131. The circuit of Claim 124, wherein the PIN or NIP steering diodes have an intrinsic "I" region of high resistivity with a long lifetime;

a highly doped p region;

an n region;

the "I" region is located between the p region and n region.

132. The circuit of Claim 131 wherein the "I" region of the PIN or NIP steering diodes have a width of between 10 and 500 μm and a resistivity of 250 ohm-cm or higher.

133. The circuit of Claim 131, wherein the PIN or NIP diode has a circular-die structure.

134. The circuit of Claim 131, wherein the PIN or NIP diode has a square die structure.

135. The circuit of Claim 131, wherein the PIN or NIP diode has a rectangular die structure.

136. The circuit of Claim 124, for use in multiple diode-leg arrays.

137. The circuit of Claim 124, comprising a PIN or NIP diode array packaged in a SOIC-8 package.

138. The circuit of Claim 124, comprising a PIN or NIP diode array packaged in an eight (8) pin dual-in-line package.

139. The circuit of Claim 124, comprising a PIN or NIP diode array packaged in a SOIC-14 package.

140. The circuit of Claim 124, comprising a PIN or NIP diode array packaged in a fourteen (14) pin dual-in-line package.

141. The circuit of Claim 124, comprising a PIN or NIP diode array provided in multiple discrete semiconductor chips.

142. The circuit of Claim 124, comprising a PIN or NIP diode array provided using multiple diode junctions diffused into a single semiconductor chip or monolithic structure.

143. The circuit of Claim 124, further comprising an array packaged with three (3) or more terminals.

144. The circuit of Claim 124, adapted for use in high frequency telecommunication lines.

145. The circuit of Claim 124, adapted for use in wireless communications devices.

146. The circuit of Claim 124, adapted for use in high baud-rate lines requiring TVS protection.

147. The circuit of Claim 124, adapted for use in multimedia systems.

148. The circuit of Claim 124, adapted for use in network applications and system designs.

149. A method of protecting sensitive components downstream in the circuit, comprising:

using PIN or NIP diodes to clamp voltages at a point upstream from sensitive components to a predetermined level;

shunting high-voltage transients to ground or to other reference points such as the positive ($+V_{CC}$) or negative ($-V_{CC}$) side of a power-supply line; and

minimizing capacitance variations with applied reverse voltage across the PIN or NIP diodes.

150. The method of Claim 149, adapted for use in high frequency telecommunication lines.

151. The method of Claim 149, adapted for use in wireless communication devices.

152. The method of Claim 149, adapted for use in high baud-rate lines requiring TVS protection.

153. The method of Claim 149, adapted for use in multimedia systems.

154. The method of Claim 149, adapted for use in network applications and system designs.